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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,617	10/18/2001	Michael R. Boyd	65783-0007	8210

10291 7590 10/18/2006

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EXAMINER

SHELEHEDA, JAMES R

ART UNIT PAPER NUMBER

2623

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action  
Before the Filing of an Appeal Brief**

Application No.

09/982,617

Applicant(s)

BOYD ET AL.

Examiner

James Sheleheda

Art Unit

2623

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 03 October 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.

6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: \_\_\_\_\_.

Claim(s) objected to: \_\_\_\_\_.

Claim(s) rejected: 1-41.

Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.

12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_

13. ☐ Other: \_\_\_\_\_.

  
CHRIS KELLEY

SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600

Continuation of 11. does NOT place the application in condition for allowance because:

In response to applicant's arguments on pages 9 and 10, as indicated in the previous rejections, Lavelle specifically discloses a digital bus, which can comprise a single wire, which will interconnect a plurality of different devices (170, 172; Figs. 1A and 1B; column 4, line 66-column 5, line 7 and column 9, line 60-column 10, line 2). The interconnection of a plurality of devices is, by definition, a network. Applicant is further provided with the appropriate pages of the IEEE 100 Dictionary, which states "a network is any set of devices or subsystems connected by links joining (directly or indirectly) a set of terminal nodes." (page 726, network (7)). Thus, applicant's argument that Lavelle does not disclose a digital data network is not persuasive. A digital bus interconnecting a plurality of devices clearly constitutes a network.

Furthermore, in regards to the "interface stage for interfacing with a digital data network", as Lavelle clearly discloses wherein the system comprises "input/output interfaces" (column 3, lines 25-43) and wherein the system "interfaces" with the digital data network (as all of the devices connect with the bus; see Figs. 1A-1B), this clearly meets the claim limitation of an interface stage for interfacing with a digital data network, thus applicant's argument is not persuasive.

In response to applicant's arguments concerning the multi-format decoder, Lavelle specifically discloses wherein signal processing/conversion facilities, 127 perform decoding (column 6, lines 28-33), and thus clearly meets the limitation of a "decoder". Furthermore, Lavelle discloses wherein the signal processing/conversion facilities, 127, can perform decoding for the inputs of any of the input devices (wherein each device is capable of it's own encoding and the facilities, 127, performs all of the decoding column 6, lines 37-42). As the inputs include a large plurality of different devices with different formats (see column 4, lines 16-30 and column 5, lines 30-42), the signal processing/conversion facilities clearly qualifies as a "multi-format decoder for decoding at least two different encoding formats for an audio-visual stream", and thus applicant's arguments are not persuasive. Furthermore, applicant's argument that all of the input devices would somehow utilize the same format is not convincing, as the devices include a DVD player, a CD player, a TV tuner, a video cassette player, an AM/FM radio and a video game player.

In response to applicant's arguments in regards to the microcontroller, Lavelle specifically discloses wherein the entire system is implemented and controlled by a computer platform consisting of a CPU, RAM and I/O. This clearly reads upon the claimed "microcontroller for controlling said interface stage and said decoder", as the computer system is running and controlling the entire system, which clearly includes the decoder/interface stage.